AMENDMENTS TO THE CLAIMS

Claims 1-12 (Cancelled)

13. (Withdrawn) A method of manufacturing a semiconductor device comprising the steps of:

forming a first gate insulating film on a main surface of a semiconductor substrate of a first conductivity type;

forming a first floating gate electrode on said first gate insulating film;

forming a first interlayer insulating film on an upper surface and a side surface of said first floating gate electrode;

forming a second gate insulating film on the main surface of said semiconductor substrate;

forming a second floating gate electrode on said first interlayer insulating film and said second gate insulating film to have a portion located above said first floating gate electrode and at least an end extended to a position on semiconductor substrate near one end of said first floating gate electrode;

forming a second interlayer insulating film at least on an upper surface of said second floating gate electrode;

forming a control gate electrode on upper surfaces of said first and second floating gate electrodes with said first and second interlayer insulating film therebetween, respectively; and

introducing impurity into said semiconductor substrate using said control gate electrode as a mask to form a first impurity region of a second conductivity type having a region

overlapping with the other end of said first floating gate electrode and a second impurity region of the second conductivity type having a region overlapping with an end of said second floating gate electrode.

14. (Withdrawn) The method of manufacturing the semiconductor device according to claim 13, wherein said first interlayer insulating film and said second gate insulating film are formed at the same step.

15. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a gate insulating film on a main surface of a semiconductor substrate of a first conductivity type;

forming first and second floating gate electrodes on said gate insulating film with a predetermined space between each other by:

forming a floating gate electrode layer on said gate insulating film, and

subsequently patterning said floating gate electrode layer using a pattern mask over the floating gate electrode layer;

forming an interlayer insulating film on upper surfaces and side surfaces of said first and second floating gate electrodes;

forming a second gate insulating film on a surface of said semiconductor substrate located between said first and second floating gate electrodes;

forming a control gate electrode on surfaces of said interlayer insulating film and said second gate insulating film;

introducing impurity into said semiconductor substrate with an end of said first floating gate electrode as a mask to form a first impurity region of second conductivity type having a region overlapping with said one end of said first floating gate electrode;

introducing impurity into said semiconductor substrate using an end of said second floating gate electrode as a mask to form a second impurity region of the second conductivity type having a region overlapping with said one end of said second floating gate electrode; and

introducing impurity into said semiconductor substrate using said first and second floating gate electrodes as a mask to form a third impurity region between the first and second floating gate electrodes, wherein

said first and second floating gate electrodes, said first and second impurity regions, and said control gate electrode constitute a common memory cell transistor.

Claim 16 (Original) The method of manufacturing the semiconductor device according to claim 15, wherein said interlayer insulating film and said second gate insulating film are formed at the same step.